CLAIMS

1. A thin film capacitive element comprising a substrate having applied thereon a capacitor structure constituted from a lower electrode, a dielectric layer formed on the lower electrode and an upper electrode formed on the dielectric layer, in which said dielectric layer comprises a high dielectric constant material represented by the following formula (I):

$$(Ba_{(1-y)(1-x)}Sr_{(1-y)x}Y_y)Ti_{1+z}O_{3+\delta}$$

wherein $0 < x < 1$, $0.007 < y < 0.02$, $-1 < \delta < 0.5$, and $(Ba_{(1-y)(1-x)}+Sr_{(1-y)x})/Ti_{1+z} < 1$.

2. The capacitive element according to claim 1 wherein said dielectric layer has a thickness of 1 to 300 nm.

3. The capacitive element according to claim 1 wherein said substrate comprises an insulating material selected from the group consisting of a glass, semiconductor material and resinous material.

4. The capacitive element according to claim 1 wherein said substrate comprises a semiconductor material or wafer.

5. The capacitive element according to claim 4 wherein said semiconductor material or wafer comprises at least one material selected from the group consisting of Si, Ge, SiGe, GaAs, InAs, InP and other compounds derived from the elements of Group III and V of the periodic table.

6. The capacitive element according to claim 1 which further comprises at least one insulating layer applied over said substrate, and said insulating layer comprises an insulating material selected from the group consisting of oxides, nitrides or oxynitrides of metal, high dielectric constant metal oxides, xerogels, organic resin and combinations or mixtures thereof.

7. The capacitive element according to claim 6 in which said insulating layer has a multilayered structure.

8. The capacitive element according to claim 1 which further comprises an adhesion layer between said substrate and said capacitor structure, and said adhesion layer comprises at least one material selected from the group consisting of noble metals, alloys of noble metals, alloys of noble and non-noble metals, conductive oxides of noble metals, insulating metal oxides, insulating metal nitrides, conducting metal nitrides, and combinations or mixtures thereof.

9. The capacitive element according to claim 1 wherein said adhesion layer comprises at least one material selected from the group consisting of Pt, Ir, Zr, Ti, TiOx, IrOx, PtOx, ZrOx, TiN, TiAlN, TaN and TaSiN in which x is a positive integer.

10. The capacitive element according to claim 8 in which said adhesion layer has a multilayered structure.

11. The capacitive element according to claim 1 wherein said lower electrode comprises at least one material selected from the group consisting of transition metals, noble metals, alloys of noble metals, alloys of noble and non-noble metals, conductive oxides and combinations or mixtures thereof.

12. The capacitive element according to claim 1 wherein said lower electrode comprises at least one material selected from the group consisting of Pt, Pd, Ir, Ru, Rh, Re, Os, Au, Ag, Cu, PtOx, IrOx and RuOx in which x is a positive integer.

13. The capacitive element according to claim 1 in which said lower electrode has a multilayered structure.

14. The capacitive element according to claim 1 in which said high dielectric constant material is a material represented by the following formula (II):

$$(Ba_{0.689}Sr_{0.296}Y_{0.015})Ti_{1+z}O_{3+\delta}$$

wherein $0.02 < z < 0.05$ and $-0.3 < \delta < 0.3$.

15. The capacitive element according to claim 1 in which said high dielectric constant material is a

material represented by the following formula (III):

$(Ba_{0.493}Sr_{0.493}Y_{0.014})Ti_{1+z}O_{3+\delta}$

wherein $0.02 < z < 0.05$ and $-0.3 < \delta < 0.3$.

16. The capacitive element according to claim 1 wherein said upper electrode comprises at least one material selected from the group consisting of transition metals, noble metals, alloys of noble metals, alloys of noble and non-noble metals, conductive oxides and combinations or mixtures thereof.

17. The capacitive element according to claim 1 wherein said upper electrode comprises at least one material selected from the group consisting of Pt, Pd, Ir, Ru, Rh, Re, Os, Au, Ag, Cu, PtOx, IrOx, RuOx, $SrRuO_3$ and $LaNiO_3$ in which x is a positive integer.

18. The capacitive element according to claim 1 in which said upper electrode has a multilayered structure.

19. The capacitive element according to claim 1 which further comprises a passivating layer on said upper electrode.

20. The capacitive element according to claim 19 in which said passivating layer comprises a silicon nitride layer.

21. The capacitive element according to claim 1 which comprises at least two capacitor structures connected in series.

22. The capacitive element according to claim 1 which comprises at least two capacitor structures connected in parallel.

23. A process for the production of a thin film capacitive element comprising a substrate having applied thereon a capacitor structure constituted from a lower electrode, a dielectric layer formed on the lower electrode and an upper electrode formed on the dielectric layer, which process comprises the steps of:

forming a lower electrode on a substrate;

forming on said lower electrode a dielectric

layer from a high dielectric constant material represented by the following formula (I):

$$(Ba_{(1-y)(1-x)}Sr_{(1-y)x}Y_y)Ti_{1+z}O_{3+\delta}$$

wherein $0 < x < 1$, $0.007 < y < 0.02$, $-1 < \delta < 0.5$, and $(Ba_{(1-y)(1-x)}+Sr_{(1-y)x})/Ti_{1+z} < 1$; and

forming on said dielectric layer an upper electrode to complete said capacitor structure.

24. The process for the production of a thin film capacitive element according to claim 23 in which said dielectric layer is formed at a thickness of 1 to 300 nm.

25. The process for the production of a thin film capacitive element according to claim 23 which further comprises the step of forming an insulating layer over said substrate.

26. The process for the production of a thin film capacitive element according to claim 23 which further comprises the step of forming an adhesion layer between said substrate and said lower electrode.

27. The process for the production of a thin film capacitive element according to claim 23 which further comprises the step of forming a passivating layer on said upper electrode.

28. The process for the production of a thin film capacitive element according to claim 23 which further comprises the step of annealing said capacitive element in an oxygen-containing ambient atmosphere at a temperature of 100 to 900°C.

29. An electronic device comprising at least one electronic element and at least one capacitive element described in any one of claims 1 to 22.

30. The electronic device according to claim 29 in which said electronic element is one member selected from the group consisting of capacitors, resistors, inductors, semiconductor elements, wirings, circuits and electrodes.